

### **REMARKS**

Claims 1-21, 23-26, and 28-42 remain pending in the present application. Claims 2 and 32 have been amended to put these claims into independent form, and should now be allowed as indicated by the Office Action (pp. 15-16). Claims 38-42 have been amended to put these claims into better form. Claims 1, 11, 21, 26, 31 and 37 have been amended to bring out difference between two memories recited in these claims. Claims 21 and 26 have been amended. Claims 22 and 27 have been previously cancelled.

#### **Claim Rejections under 35 U.S.C. § 112, Second Paragraph**

Claims 21 and 26 were rejected under 35 U.S.C. § 112, second paragraph as failing to distinctly claim the invention. In particular, the Office Action objects to the phrase “for quick access.” The claims have been amended by deleting this phrase. Accordingly, reconsideration and withdrawal of the rejection of claims 21 and 26 under 35 U.S.C. § 112, second paragraph is respectfully requested.

#### **Claim Rejections under 35 U.S.C. § 103(a)**

Claims 1, 3-9, 11-19, 21, 23-31, 33-35, and 37-41 were rejected were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,630,083 to Carbine (“Carbine”) in view of U.S. Patent No. 5,765,220 to Kipp (“Kipp”). Claims 10, 20, 36 and 42 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Carbine and Kipp in view of “common art.”

According to an embodiment of the present invention, a micro-operation cache and micro-operation memory are provided to store micro-operation information. For example, the

micro-operation cache may store the most commonly used micro-operations that are stored in the micro-operation memory. The trace pipe receives micro-operation information from both the micro-operation memory and the micro-operation cache. A potential advantage of this configuration is that all micro-operation information would come from a single structure, instead of receiving information for short instructions from programmable logic arrays ("PLAs") and receiving information for long instructions from a UROM.

In rejecting the claims based on Carbine, the Office Action cites to the American Heritage Dictionary to support a conclusion that a ROM should be interpreted as a cache. Carbine, however, does not show a cache, and instead provides the UROM. The rejection of claim 1 appears to be that the UROM of Carbine shows the micro-operation cache and the micro-operation memory recited in the claim. Claim 1 has been amended to bring out what was implicit in the claim before amendment, the micro-operation cache and the micro-operation memory are two distinct elements of the claim. Claim 1 recites that the micro-operation cache is to store a subset of micro-operations to be stored in the micro-operation memory. A similar amendment has been made to claims 11, 21, 26, and 31.

As stated in the prior Amendment, Carbine refers to a decoder for decoding multiple instructions in parallel and does not show a micro-operation cache as recited in the independent claims. Kipp was cited to allegedly show the use of an instruction pointer queue, but does not make up for the deficiencies of Carbine. Kipp provides a cache for storing instruction addresses, but does not show the memory/cache limitations for storing micro-operations as recited in the claims.

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Since features of the claims are neither taught nor suggested by Carbine and/or Kipp, reconsideration and withdrawal of the rejection of claims 1, 3-21, 23-26, 28-31, and 33-41 under 35 U.S.C. § 103(a) is respectfully requested.

### CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,  
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